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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,008	03/23/2001	Richard E. Pekkala	BAN:0107	5720

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HUFFMAN LAW GROUP, P.C.
1900 MESA AVE.
COLORADO SPRINGS, CO 80906

EXAMINER	
DOAN, DUYEN MY	

ART UNIT	PAPER NUMBER
2152	

NOTIFICATION DATE	DELIVERY MODE
07/25/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO@HUFFMANLAW.NET

Office Action Summary	Application No.	Applicant(s)	
	09/817,008	PEKKALA ET AL.	
	Examiner	Art Unit	
	Duyen M. Doan	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-113* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-113* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the submission filed on 5/9/2007. Claims 1-113 are presented for examination.

Response to Arguments

The affidavit filed on 5/9/2007 have been reviewed and accepted by the examiner.

Applicant's arguments with respect to claims 1-113 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "said plurality of InfiniBand Mac". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-113 rejected under 35 U.S.C. 103(a) as being unpatentable over Baumert et al (us pat 6,067,300) (hereinafter Bau) in view of Brian et al (us pat 6,658,521) (hereinafter Brian).

As regarding claim 1, Bau discloses a plurality of media access controllers (MACs), for transceiving packets (see Bau col.1, line 38-41, figure 1, Macs 18); a local bus interface, for performing addressed data transfers on a local bus coupled thereto (see Bau col.3, line 64-67; col.4, lines 1-5); a memory, shared by said plurality of MACs, said local bus interface, and said bus router, for buffering data received thereby (see Bau col.3, line 6-7); and a transaction switch, coupled to each of said memory, said plurality of MACS, said local bus interface and said bus router, for switching data and transactions therebetween (see Bau col.3, lines 13-20, figure 1, switch controller 23).

Brian does not explicitly disclose a bus router, for performing transport layer operations between interfaces. However a bus router for performing transport layer

operations is well known, for instant Brian teaches a bus router, for performing transport layer operations between interfaces (see Brian col.3, lines 52-67).

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the teaching of Brian to the system of Bau to include a bus router for performing transport layer operations for the purpose of allowing different devices communicate with each other (see Brian col.2, lines 5-26).

As regarding claim 2, Bau-Brian discloses a plurality of transaction queues, associated with said plurality of MACs, said local bus interface, and said bus router, coupled to said transaction switch, for storing said transaction (see Bau, col.3, lines 4-9).

As regarding claim 3, Bau-Brian discloses a random access memory (see Bau col.3, line 8).

As regarding claim 4, Bau-Brian discloses a buffer manager, for allocating portions of said memory to said plurality of MACs, said local bus interface and said bus router, for buffering said data received thereby (see Bau col.3, lines 12-20).

As regarding claim 5, Bau-Brian discloses buffer manager performs said allocating in an as-needed manner (see Bau col.3, lines 12-20).

As regarding claim 6, Bau-Brian discloses said bus router is configured to write packet header into said memory via said transaction switch along with addressed data stored in said memory by said local bus interface to create packet (see Bau col.3, lines 14-28).

As regarding claim 7, Bau-Brian discloses local bus interface configured to read a payload portion of packet stored in said memory and to transmit said payload portion on said local bus coupled thereto (see Bau col.3, lines 14-28).

As regarding claim 8, Bau-Brian discloses said payload portion is located in said memory at an offset specified in a transaction posted by said bus router to said local bus interface via said transaction switch (see Brian col.2, lines 5-26). The same motivation was utilized in claim 1 applied equally well to claim 9.

As regarding claim 9, Bau-Brian discloses wherein said local bus interface comprises a PCI interface (see Brian col.2, lines 5-26). The same motivation was utilized in claim 1 applied equally well to claim 9.

As regarding claim 10, Bau-Brian discloses transaction switch is configured to receive a transaction posted by a first of said plurality of MACs in response to a packet received by said first of said plurality of MACs and to selectively witch said transaction

to one of a second of said plurality of MACs and said bus router (see Bau col.5, lines 52-67).

As regarding claim 11, Bau-Brian discloses transaction switch selectively switches said transaction based on an Infiniband destination local identification value included in said transaction (see Brian col.2, lines 5-26). The same motivation was utilized in claim 1 applied equally well to claim 11.

As regarding claim 12, Bau-Brian discloses transaction switch selectively switches said transaction to said bus router if an entry associated with said InfiniBand destination local identification value in a mapping table of said transaction switch indicates said transaction is destined for said bus router (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 12.

As regarding claim 13, Bau-Brian discloses said transaction switch selectively switches said transaction to one of said plurality of InfiniBand MACs based on which of said plurality of InfiniBand MACs is associated with said InfiniBand destination local identification value in said mapping table if said entry indicates said transaction is not destined for said bus router (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 13.

As regarding claim 14, Bau-Brian discloses first MAC parses said InfiniBand destination local identification value from said packet (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 14.

As regarding claim 15, Bau-Brian discloses transaction includes an InfiniBand virtual lane number parsed from said packet (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 15.

As regarding claim 16, Bau-Brian discloses transaction includes a destination queue pair number parsed from said packet (see Brian col.4, lines 15-52). The same motivation was utilized in claim 1 applied equally well to claim 16.

As regarding claim 17, Bau-Brian discloses transaction switch is configured to receive a transaction posted by said bus router and to selectively switch said transaction to one of said plurality of MACs and said local bus interface (see Bau col.3, lines 1-21).

As regarding claim 18, Bau-Brian discloses transaction switch selectively switches said transaction based on a transaction type value included in said transaction (see Bau col.3, lines 1-21).

As regarding claim 19, Bau-Brian discloses a second local bus interface for performing addressed data transfers on a second local bus coupled thereto; wherein said transaction switch selectively switches said transaction to one of said first and second local bus interfaces based on whether a local bus address included in said transaction falls into one or more predetermined address ranges of said first and second buses (see Bau col.3, lines 57-67; col.4, lines 1-25).

As regarding claim 20, Bau-Brian discloses said transaction includes an address in an address range of said local bus (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 20.

As regarding claim 21, Bau-Brian discloses a second local bus interface for performing addressed data transfers on a second local bus coupled thereto; a local bus bridge coupled between said first and second local bus interfaces for buffering data therebetween (see Bau col.4, lines 1-25).

As regarding claim 22, Bau-Brian discloses a second bus interface; wherein said transaction switch is configured to receive a transaction posted by said first local bus interface in response to an addressed data transfer received by said first local bus interface and to switch said transaction to second local bus interface (see Bau, col.3, lines 1-21, lines 57-67).

As regarding claim 83, Bau-Brian discloses wherein at least one of said plurality of MACs comprises an Infiniband MAC (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 83.

As regarding claim 84, Bau-Brian discloses wherein at least one of said plurality of MACs comprises an Ethernet MAC (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 84.

As regarding claim 93, Bau-Brian discloses wherein at least one of said plurality of addressed data devices comprises an interface to a bus for coupling to a random access memory (see Bau col.3, line 8).

As regarding claim 23, Bau-Brian discloses a memory, shared by the plurality of data devices for buffering data received thereby (see Bau fig.2, memory 20-22); multiplexing logic, for controlling the transfer of data between the plurality of data devices and said memory (see Bau fig.2, element 51); and control logic, for controlling said multiplexing logic (see Bau col.4, lines 1-24); wherein the plurality of data devices comprise a plurality of packetized data devices and a plurality of addressed data devices (see Brian col.2, lines 5-29); wherein said control logic is configured to selectively control said multiplexing logic to transfer data through said memory between two of said packetized data devices and between one of said packetized data devices

and one of said addressed data devices (see Brian col.2, lines 5-29). The same motivation was utilized in claim 1 applied equally well to claim 23.

As regarding claim 24, Bau-Brian discloses wherein said control logic is further configured to selectively control said multiplexing logic to transfer data through said memory between two of said addressed data devices (see Brian col.2, lines 5-29). The same motivation was utilized in claim 1 applied equally well to claim 24.

As regarding claim 25, Bau-Brian discloses wherein said control logic is configured to selectively control said multiplexing logic to transfer data through said memory between two of said packetized data devices and between one of said packetized data devices and one of said addressed data devices concurrently (see Brian col.2, lines 5-29). The same motivation was utilized in claim 1 applied equally well to claim 25.

As regarding claim 26, Bau-Brian discloses wherein at least two of said packetized data devices comprise InfiniBand interfaces (see Brian col.2, lines 5-29). The same motivation was utilized in claim 1 applied equally well to claim 26.

As regarding claim 27, Bau-Brian discloses wherein at least two of said addressed data devices comprise PCI bus interfaces (see Brian col.2, lines 5-29). The same motivation was utilized in claim 1 applied equally well to claim 27.

As regarding claim 28, Bau-Brian discloses a buffer manager, for allocating portions of said memory to the plurality of data devices for buffering said data (see Brian col.3, lines 13-43. The same motivation was utilized in claim 1 applied equally well to claim 28.

As regarding claim 29, Bau-Brian discloses wherein buffer manager is configured to perform said allocating on substantially a first-come-first-serve basis (see Brian col.3, lines 13-43. The same motivation was utilized in claim 1 applied equally well to claim 29.

As regarding claim 30, Bau-Brian discloses said control logic is configured to selectively control said multiplexing logic to transfer data through said memory between two of said packetized data devices and between one of said packetized data devices and one of said addressed data devices in response to a transaction posted to the transaction switch by the plurality of data devices (see Brian col.3, lines 13-43. The same motivation was utilized in claim 1 applied equally well to claim 30.

As regarding claim 31, Bau-Brian discloses transaction comprises a command to transfer data between said memory and one of the plurality of data devices (see Brian col.3, lines 13-43. The same motivation was utilized in claim 1 applied equally well to claim 31.

As regarding claim 32, Bau-Brian discloses wherein said transaction comprises an address of a buffer within said memory wherein is stored said data to be transferred in response to said command (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 32.

As regarding claim 33, Bau-Brian discloses transaction comprises an offset within said buffer for addressing portions of said data (see Brian col.2, lines 5-29). The same motivation was utilized in claim 1 applied equally well to claim 33.

As regarding claim 34, Bau-Brian discloses wherein said transaction comprises a tag for uniquely identifying said transaction from other transactions posted to the transaction switch by the plurality of data devices (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 34.

As regarding claim 35, Bau-Brian discloses wherein the plurality of data devices comprise a transport layer device, wherein the transaction switch is configured to receive transactions from said transport layer device for performing protocol translation of data between said one of said packetized data devices and said one of said addressed data devices (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 35.

As regarding claim 80, Bau-Brian discloses wherein a single integrated circuit comprises the transaction switch (see Bau col.3, lines 13-28).

As regarding claim 85, Bau-Brian discloses wherein at least one of said at least two of said packetized data devices comprise an Ethernet interface (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 32.

As regarding claim 94, Bau-Brian discloses wherein at least one of said plurality of addressed data devices comprises an interface to a bus for coupling to a random access memory (see Bau col.3, line 8).

As regarding claims 36-40,81,86,95, limitations are similar to limitations of rejected claims 23-35,80,85,94, therefore rejected for the same rationale.

As regarding claims 41-62,87,96, the limitations are similar to limitations of rejected claims 1-22,83-84,93, therefore rejected for the same rationales. Bau-Brian further discloses at least three interfaces, and at least one of said at least three data interfaces is of a different type that the others (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 41.

As regarding claims 63-66,88-89,97, the limitations are similar to limitations of rejected claims 41-62,87,96, 83 therefore rejected for the same rationales.

As regarding claims 67-70,82,90-91,98, the limitations are similar to limitations of rejected claims 1-22,83-84,93, therefore rejected for the same rationales.

As regarding claims 71-78,92,99, the limitations are similar to limitations of rejected claims 1-22,83-84,93, therefore rejected for the same rationales.

As regarding claim 79, the limitations are similar to limitations of rejected claims 23-65,80,85,94, therefore rejected for the same rationale.

As regarding claim 100, Bau-Brian discloses invention substantially as claimed in claim 1, Bau-Brian further discloses wherein the transport protocol engine is configured to perform the protocol translation before the MAC reads the packet from the memory for transmission on the network, wherein the transport protocol engine performs the protocol translation without copying the data to another memory (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 100.

As regarding claim 101, Bau-Brian discloses wherein the transport protocol engine is further configured to perform second protocol translation from the packetized data protocol to the addressed data protocol by identifying a data payload within a second packet received from the network by the MAC and specifying a local bus address for the data payload (see Brian col.3, lines 13-43); wherein the transport

protocol engine is further configured to perform the second protocol translation before the local bus interface reads the data payload from the memory for writing on the local bus to the local bus address, wherein the transport protocol engine performs the second protocol translation within the memory without copying the data to another memory see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 101.

As regarding claim 102, Bau-Brian discloses wherein a single integrated circuit comprises the local bus interface, the MAC, the transport protocol engine, the memory, and the transaction switch (see Bau col.3, lines 1-39).

As regarding claim 103, Bau-Brian discloses wherein the transport protocol engine is configured to create the packet by writing a packet header into the memory in front of the data (see Brian col.3, lines 13-43). The same motivation was utilized in claim 1 applied equally well to claim 103.

As regarding claims 104-107, the limitations are similar to limitations of claims 100-103, therefore rejected for the same rationale as claims 100-103.

As regarding claims 108-110, the limitations are similar to limitations of claims 100-103, therefore rejected for the same rationale as claims 100-103.

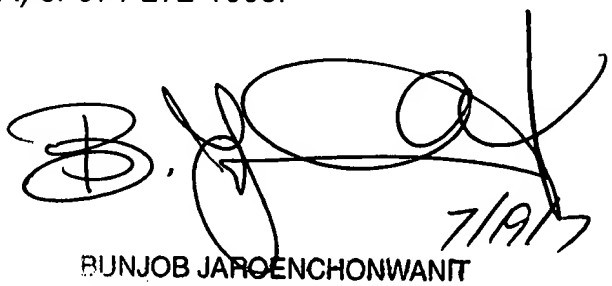
As regarding claims 111-113, the limitations are similar to limitations of rejected claims 100-103, therefore rejected for the same rationale.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duyen M. Doan whose telephone number is (571) 272-4226. The examiner can normally be reached on 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on (571) 272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner
Duyen Doan
Art unit 2152



BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER